WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a metal gate electrode, having top, bottom and side surfaces, over a substrate with a gate dielectric layer therebetween, wherein the metal gate electrode comprises:

a layer of tantalum nitride forming the bottom and side surfaces of the metal gate electrode, the layer of tantalum nitride having a nitrogen content that increases from the gate dielectric layer toward the top surface.

2. The semiconductor device according to claim 1, wherein the metal gate electrode further comprises a metal layer on the layer of tantalum nitride.

3. The semiconductor device according to claim 1, wherein the metal is copper (Cu) or a Cu alloy.

4. The semiconductor device according to claim 2, wherein the nitrogen content varies from 10 at.% proximate the gate dielectric layer upwardly to a nitrogen content of 70 at.%.

5. The semiconductor device according to claim 2, wherein the metal gate electrode comprises a single layer of tantalum nitride having a graded nitrogen content varying from 10 at.% to 70 at.%.

6. The semiconductor device according to claim 5, wherein the layer of tantalum nitride has a thickness of 15 Å to 25 Å.

7. The semiconductor device according to claim 2, wherein the metal gate electrode comprises a plurality of layers of tantalum nitride having each layer having a nitrogen content greater than that of an immediately underlying layer.

8. The semiconductor device according to claim 7, wherein each layer of tantalum nitride has a thickness of 15 Å to 25 Å.

9. The semiconductor device according to claim 7, wherein the metal gate electrode comprises:

a first layer of tantalum nitride having a nitrogen content of 15 at.% to 25 at.% on the gate dielectric layer;

a second layer of tantalum nitride having a nitrogen content of 40 at.% to 70 at.% on the first layer of tantalum nitride; and

a third layer of tantalum nitride having a nitrogen content of 60 at.% to 80 at.%, on the second layer of tantalum nitride.

10. A method of manufacturing a semiconductor device having a transistor with a metal gate electrode, the metal gate electrode having upper and lower surfaces, the method comprising:

forming a removable gate over a substrate with a gate dielectric layer therebetween;

forming a dielectric layer over the substrate and exposing an upper surface of the removable gate;

removing the removable gate leaving an opening in the dielectric layer, the opening defined at its bottom by the gate dielectric layer and defined at its sides by exposed surfaces of the dielectric layer;

deposing at least one conductive layer, having a work function, on the gate dielectric layer lining the opening;

modifying the work function of the conductive layer by creating an intrinsic electric field therein; and

depositing a metal on the conductive layer with the modified work function filling the opening.

11. The method according to claim 10, comprising annealing to activate source/drain extensions and source/drain regions before depositing the conductive layer.

12. The method according to claim 10, comprising depositing a single layer of tantalum nitride; and

modifying the work function by varying the nitrogen contents such that it gradually increases from proximate the gate dielectric layer toward the upper surface by controlling the flow of nitrogen while depositing the tantalum nitride layer.

13. The method according to claim 12, comprising forming the tantalum nitride layer at a thickness of 15 Å to 25 Å.

14. The method according to claim 12, comprising varying the nitrogen content such that it gradually increases from 10 at.% proximate the gate dielectric layer upwardly to 70 at.%.

15. The method according to claim 10, comprising forming a plurality of tantalum nitride layers, each layer having a nitrogen content greater than that of an underlying tantalum nitride layer.

16. The method according to claim 15, comprising:

depositing a first layer of tantalum nitride, having a nitrogen content of 15 at.% to 25 at.%, on the gate dielectric layer;

depositing a second layer of tantalum nitride, having a nitrogen content of 40 at.% to 70 at.%, on the first tantalum nitride layer; and

depositing a third tantalum nitride layer, having a nitrogen content of 60 at.% to 80 at.%, on the second tantalum nitride layer.

17. The method according to claim 12, further comprising forming an impurity doped layer on the layer of tantalum nitride.

18. The method according to claim 10, comprising modifying the work function of the conductive layer by introducing a dopant impurity into a surface thereof.

19. The method according to claim 10, comprising depositing a plurality of metal layers and annealing to form an alloy thereof.

20. The method according to claim 10, comprising depositing a barrier layer in the opening before depositing the conductive layer.